# DALLAS SEMICONDUCTOR

#### FEATURES

- Real-Time Clock Keeps Track of Hundredths of Seconds, Seconds, Minutes, Hours, Days, Date of the Month, Months, and Years
- 8k x 8 NV SRAM Directly Replaces Volatile Static RAM or EEPROM
- Embedded Lithium Energy Cell Maintains Calendar Operation and Retains RAM Data
- Watch Function is Transparent to RAM Operation
- Month and Year Determine the Number of Days in Each Month; Valid Up to 2100
- Lithium Energy Source is Electrically Disconnected to Retain Freshness Until Power is Applied for the First Time
- Standard 28-Pin JEDEC Pinout
- Full ±10% Operating Range
- 0°C to +70°C Operating Temperature Range
- Accuracy is Better than ±1 Minute/Month at +25°C
- Over 10 Years of Data Retention in the Absence of Power
- Available in 120ns and 150ns Access Time
- Underwriters Laboratory (UL) Recognized
- Available in Lead-Free Package

#### **ORDERING INFORMATION**

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
DS1243Y	$0^{\circ}$ C to $+70^{\circ}$ C	28 EMOD (0.720a)	DS1243Y
DS1243Y-120	$0^{\circ}$ C to $+70^{\circ}$ C	28 EMOD (0.720a)	DS1243Y-120
DS1243Y-150	$0^{\circ}$ C to $+70^{\circ}$ C	28 EMOD (0.720a)	DS1243Y-150
DS1243Y-120+	$0^{\circ}$ C to $+70^{\circ}$ C	28 EMOD (0.720a)	DS1243Y-120+

+ Denotes a lead-free/RoHS-compliant device.

## **PIN CONFIGURATION**

TOP VIEW			
RST	1	28	
A12	<sup>2</sup> <b>DS1243Y</b>	27	WE
A7	3 0512431	26	N.C.
A6	4	25 🔲	A8
A5	5	24 🛯	A9
A4	6	23	A11
A3	7	22	OE
A2	8	21	A10
A1	9	20	CE
A0	10	19 🛯	DQ7
DQ0	11	18	DQ6
DQ1	12	17	DQ5
DQ2	13	16	DQ4
GND	14	15 🗖	DQ3

Encapsulated Package (720-Mil Extended)

#### **PIN DESCRIPTION**

PIN	NAME	FUNCTION
1	RST	Active-Low Reset Input. This pin has an internal pullup resistor connected to $V_{CC}$ .
2	A12	
3	A7	
4	A6	
5	A5	
6	A4	
7	A3	
8	A2	Address Inputs
9	A1	
10	A0	
23	A11	
21	A10	
24	A9	
25	A8	
11	DQ0	
12	DQ1	
13	DQ2	
15	DQ3	Data In/Data Out
16	DQ4	
17	DQ5	
18	DQ6	
19	DQ7	
20	CE	Active-Low Chip-Enable Input
22	ŌĒ	Active-Low Output-Enable Input
26	N.C.	No Connection
27	WE	Active-Low Write-Enable Input
28	V <sub>CC</sub>	Power-Supply Input
14	GND	Ground

#### DESCRIPTION

The DS1243Y 64K NV SRAM with Phantom Clock is a fully static nonvolatile RAM (organized as 8192 words by 8 bits) with a built-in real time clock. The DS1243Y has a self-contained lithium energy source and control circuitry, which constantly monitors  $V_{CC}$  for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent corrupted data in both the memory and real time clock. The Phantom Clock provides timekeeping information including hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including correction for leap years. The Phantom Clock operates in either 24-hour or 12-hour format with an AM/PM indicator.

## **ABSOLUTE MAXIMUM RATINGS**

Voltage Range on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature Range	$\dots 0^{\circ}C$ to $+70^{\circ}C$ (noncondensing)
Storage Temperature Range	40°C to +70°C (noncondensing)
Soldering Temperature	

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

## **RECOMMENDED DC OPERATING CONDITIONS**

 $(T_A = 0^{\circ}C \text{ to } +70^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	ТҮР	MAX	UNITS	NOTES
Power Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V	
Input Logic 1	V <sub>IH</sub>	2.2		$V_{CC}$ +0.3	V	
Input Logic 0	V <sub>IL</sub>	-0.3		+0.8	V	

#### **DC ELECTRICAL CHARACTERISTICS**

 $(V_{CC} = 5V \pm 10\%, T_A = 0^{\circ}C \text{ to } +70^{\circ}C.)$ 

PARAMETER	SYMBOL	MIN	ТҮР	MAX	UNITS	NOTES
Input Leakage Current	I <sub>IL</sub>	-1.0		+1.0	μΑ	12
$\frac{I/O \text{ Leakage Current}}{CE} \ge V_{IH} \le V_{CC}$	I <sub>IO</sub>	-1.0		+1.0	μΑ	
Output Current @ 2.4V	I <sub>OH</sub>	-1.0			mA	
Output Current @ 0.4V	I <sub>OL</sub>	2.0			mA	
Standby Current $\overline{CE} = 2.2$	I <sub>CCS1</sub>		5.0	10	mA	
Standby Current $\overline{CE} = V_{CC} - 0.5V$	I <sub>CCS2</sub>		3.0	5.0	mA	
Operating Current $t_{CYC} = 200$ ns	I <sub>CC01</sub>			85	mA	
Write Protection Voltage	V <sub>TP</sub>	4.25		4.5	V	

#### **DC TEST CONDITIONS**

Outputs are open; all voltages are referenced to ground.

## CAPACITANCE

(T<sub>A</sub> = +25°C)

PARAMETER	SYMBOL	MIN	ТҮР	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>		5	10	pF	
Input/Output Capacitance	C <sub>I/O</sub>		5	10	pF	

# MEMORY AC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	DS124	3Y-120	DS124	3Y-150	DS1	243Y	UNITS	NOTES
<b>FAKANILIEK</b>	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNIIS	NULES
Read Cycle Time	t <sub>RC</sub>	120		150		200		ns	
Access Time	t <sub>ACC</sub>		120		150		200	ns	
OE to Output Valid	$t_{OE}$		60		70		100	ns	
$\overline{\text{CE}}$ to Output Valid	t <sub>CO</sub>		120		150		200	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t <sub>COE</sub>	5		5		5		ns	5
Output High-Z from Deselection	t <sub>OD</sub>		40		70		100	ns	5
Output Hold from Address Change	t <sub>oH</sub>	5		5		5		ns	
Write Cycle Time	t <sub>WC</sub>	120		150		200		ns	
Write Pulse Width	t <sub>WP</sub>	90		100		150		ns	3
Address Setup Time	t <sub>AW</sub>	0		0		0		ns	
Write Recovery Time	t <sub>WR</sub>	20		20		20		ns	
$\frac{\text{Output High-Z from}}{\overline{\text{WE}}}$	$t_{\rm ODW}$		40		70		80	ns	5
$\frac{\text{Output Active from}}{\text{WE}}$	t <sub>OEW</sub>	5		5		5		ns	5
Data Setup Time	t <sub>DS</sub>	50		60		80		ns	4
$\frac{\text{Data Hold Time from}}{\text{WE}}$	t <sub>DH</sub>	20		20		20		ns	4

# AC TEST CONDITIONS

Output Load: 50pF + 1TTL Gate Input Pulse Levels: 0 to 3V

Timing Measurement Reference Levels Input: 1.5V Output: 1.5V Input Pulse Rise and Fall Times: 5ns

## PHANTOM CLOCK AC ELECTRICAL CHARACTERISTICS

 $(V_{CC} = 4.5V \text{ to } 5.5V, T_A = 0^{\circ}C \text{ to } +70^{\circ}C.)$ 

PARAMETER	SYMBOL	MIN	ТҮР	MAX	UNITS	NOTES
Read Cycle Time	t <sub>RC</sub>	120			ns	
CE Access Time	t <sub>co</sub>			100	ns	
OE Access Time	t <sub>OE</sub>			100	ns	
$\overline{\text{CE}}$ to Output Low-Z	t <sub>COE</sub>	10			ns	
$\overline{\text{OE}}$ to Output Low-Z	t <sub>OEE</sub>	10			ns	
CE to Output High-Z	t <sub>OD</sub>			40	ns	5
OE to Output High-Z	t <sub>ODO</sub>			40	ns	5
Read Recovery	t <sub>RR</sub>	20			ns	
Write Cycle Time	t <sub>WC</sub>	120			ns	
Write Pulse Width	$t_{WP}$	100			ns	
Write Recovery	t <sub>WR</sub>	20			ns	10
Data Setup Time	t <sub>DS</sub>	40			ns	11
Data Hold Time	t <sub>DH</sub>	10			ns	11
CE Pulse Width	t <sub>CW</sub>	100			ns	
RESET Pulse Width	t <sub>RST</sub>	200			ns	
CE High to Power-Fail	t <sub>PF</sub>			0	ns	

#### **POWER-DOWN/POWER-UP TIMING**

PARAMETER	SYMBOL	MIN	ТҮР	MAX	UNITS	NOTES
$\overline{\text{CE}}$ at V <sub>IH</sub> before Power-Down	$t_{PD}$	0			μs	
$V_{CC}$ Slew from 4.5V to 0V ( $\overline{CE}$ at $V_{IH}$ )	t <sub>F</sub>	300			μs	
$V_{CC}$ Slew from 0V to 4.5V ( $\overline{CE}$ at $V_{IH}$ )	t <sub>R</sub>	0			μs	
$\overline{\text{CE}}$ at V <sub>IH</sub> after Power-Up	t <sub>REC</sub>			2	ms	

 $(T_A = +25^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	ТҮР	MAX	UNITS	NOTES
Expected Data-Retention Time	t <sub>DR</sub>	10			years	9

WARNING: Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery-backup mode.

# NOTES:

- 1.  $\overline{\text{WE}}$  is high for a read cycle.
- 2.  $\overline{OE} = V_{IH}$  or  $V_{IL}$ . If  $\overline{OE} = V_{IH}$  during write cycle, the output buffers remain in a high impedance state.
- 3.  $t_{WP}$  is specified as the logical AND of  $\overline{CE}$  and  $\overline{WE}$ .  $t_{WP}$  is measured from the latter of  $\overline{CE}$  or  $\overline{WE}$  going low to the earlier of  $\overline{CE}$  or  $\overline{WE}$  going high.
- 4.  $t_{DH}$ ,  $t_{DS}$  are measured from the earlier of  $\overline{CE}$  or  $\overline{WE}$  going high.
- 5. These parameters are sampled with a 50pF load and are not 100% tested.
- 6. If the  $\overline{CE}$  low transition occurs simultaneously with or later than the  $\overline{WE}$  low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
- 7. If the  $\overline{CE}$  high transition occurs prior to or simultaneously with the  $\overline{WE}$  high transition, the output buffers remain in a high impedance state during this period.
- 8. If  $\overline{WE}$  is low or the  $\overline{WE}$  low transition occurs prior to or simultaneously with the  $\overline{CE}$  low transition, the output buffers remain in a high impedance state during this period.
- 9. The expected  $t_{DR}$  is defined as cumulative time in the absence of  $V_{CC}$  with the clock oscillator running.
- 10.  $t_{WR}$  is a function of the latter occurring edge of  $\overline{WE}$  or  $\overline{CE}$ .
- 11.  $t_{DH}$  and  $t_{DS}$  are a function of the first occurring edge of  $\overline{\rm WE}\,$  or  $\overline{\rm CE}$  .
- 12. RST (Pin1) has an internal pull-up resistor.
- 13. Real-Time Clock Modules can be successfully processed through conventional wave-soldering techniques as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. Post-solder cleaning with water washing techniques is acceptable, provided that ultrasonic vibration is not used.